

The diagram illustrates a multi-channel system architecture. It features three parallel processing paths. Each path starts with a **CONTROL** block (labeled 20) which is connected to a **PXC** block (labeled 10). The **PXC** blocks are interconnected in series via a central line (labeled 30) that passes through three triangular components (labeled 60). Additionally, each **PXC** block is connected to a common output line (labeled 40). The diagram uses various reference numerals to identify components and connections: 10 for PXC blocks, 20 for CONTROL blocks, 30 for the central line, 40 for the output line, 50 for the input/output ports of the PXC blocks, and 60 for the triangular components.

FIG. 1A, PRIOR ART

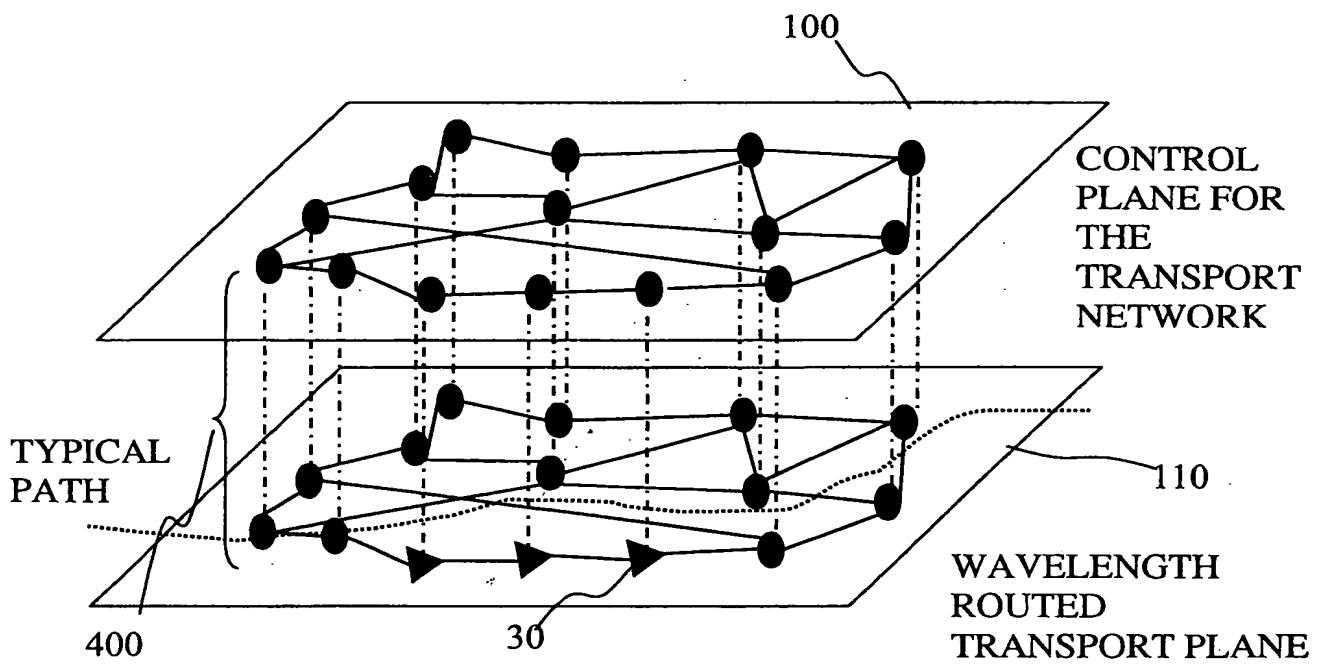


FIG. 1B, PRIOR ART

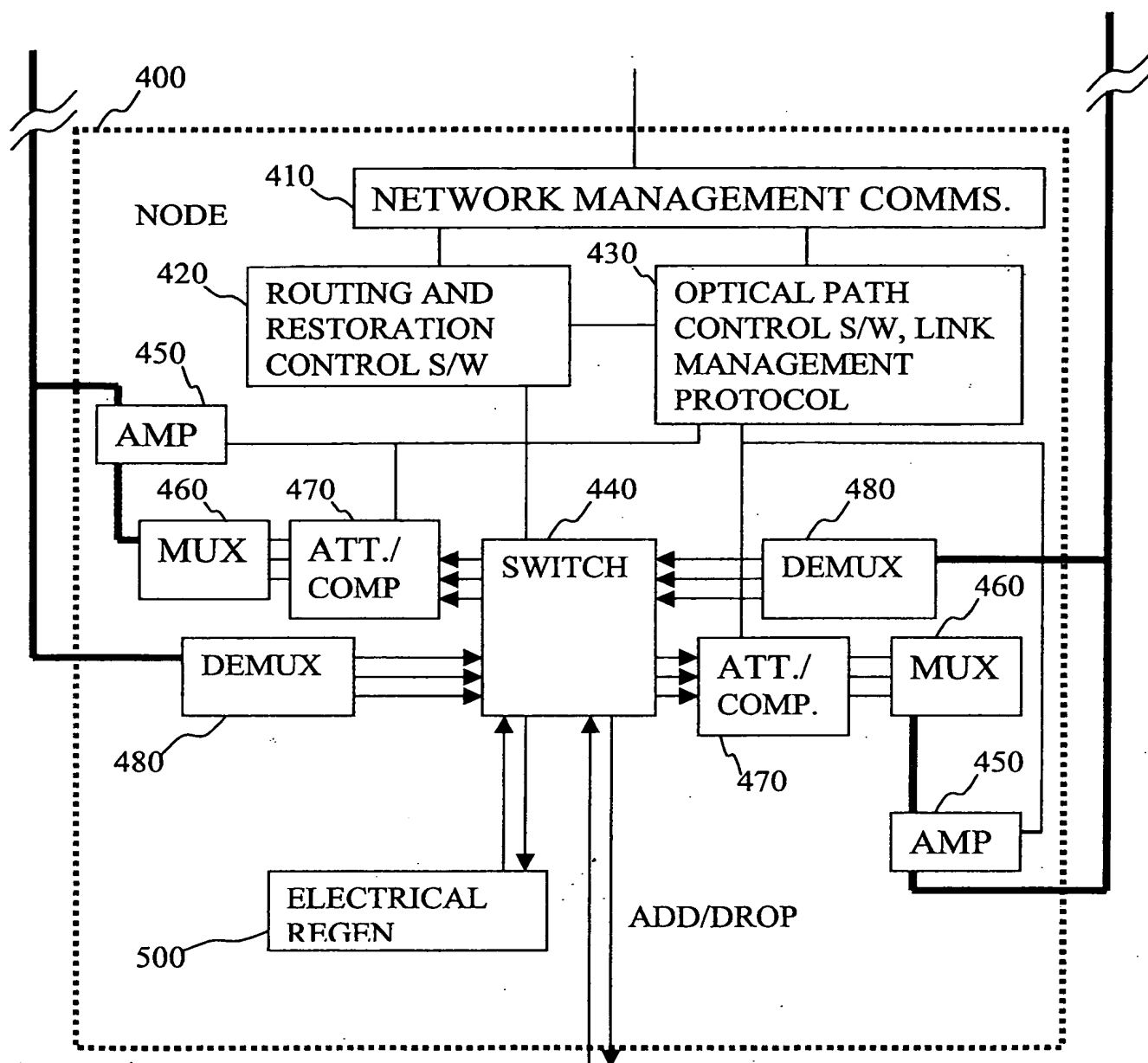


FIG. 2, PRIOR ART, OVERALL SCHEMATIC VIEW OF A
NODE FOR USE IN THE WAVELENGTH ROUTED MESH
NETWORK OF FIG. 1A OR 1B.

FIG. 3

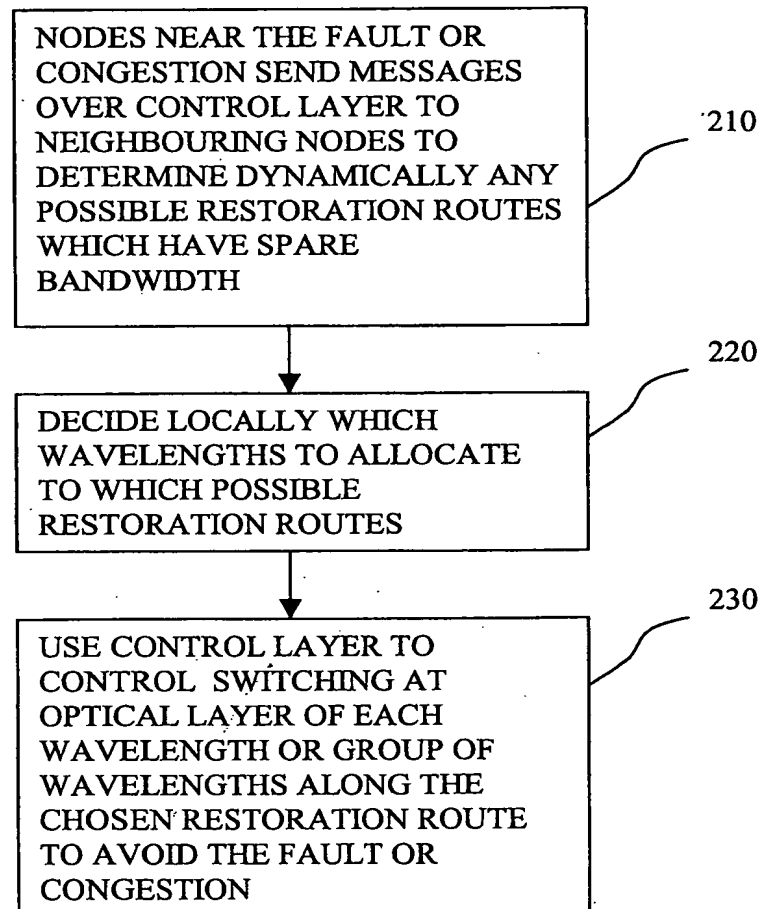


FIG. 4

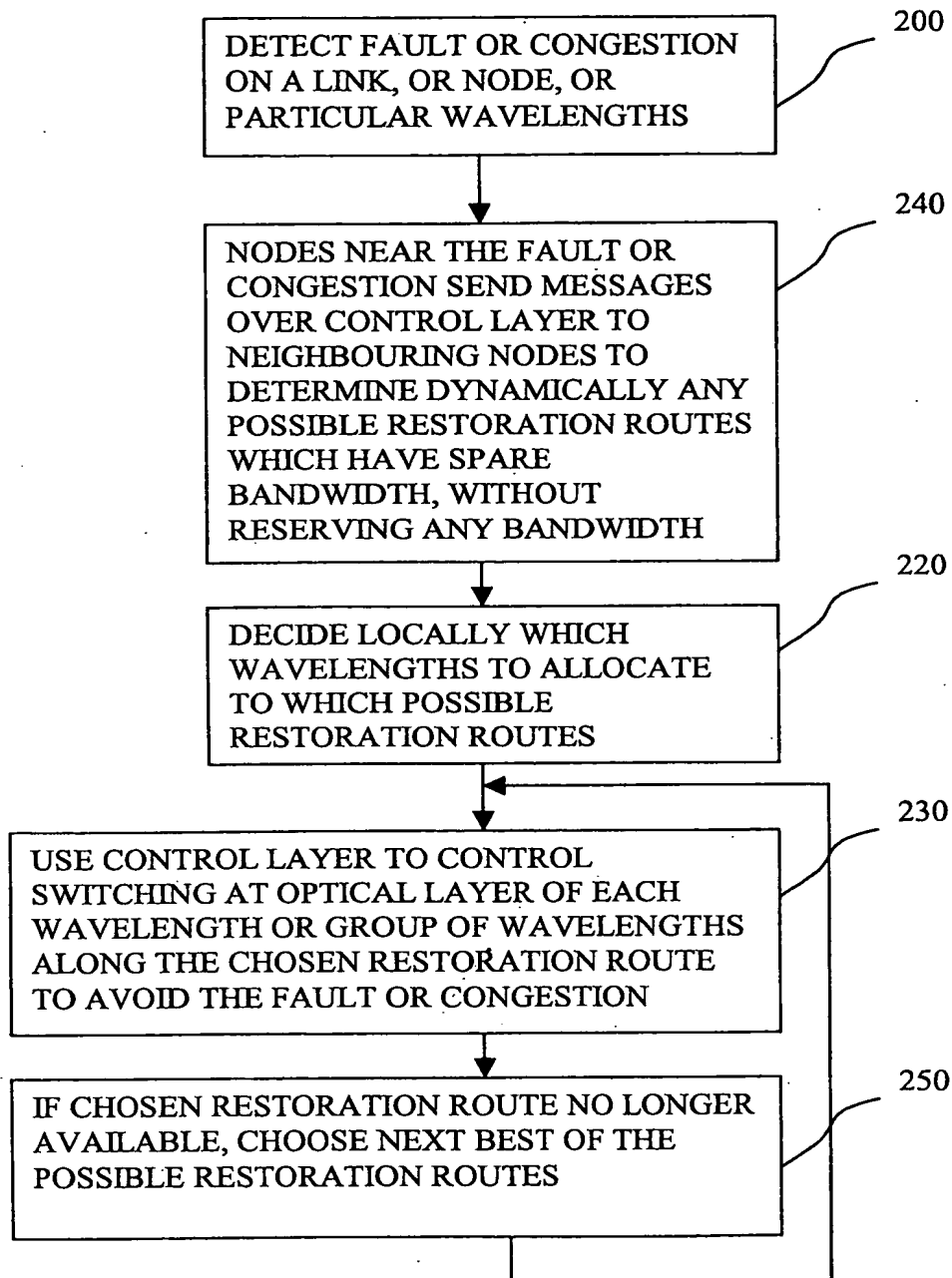
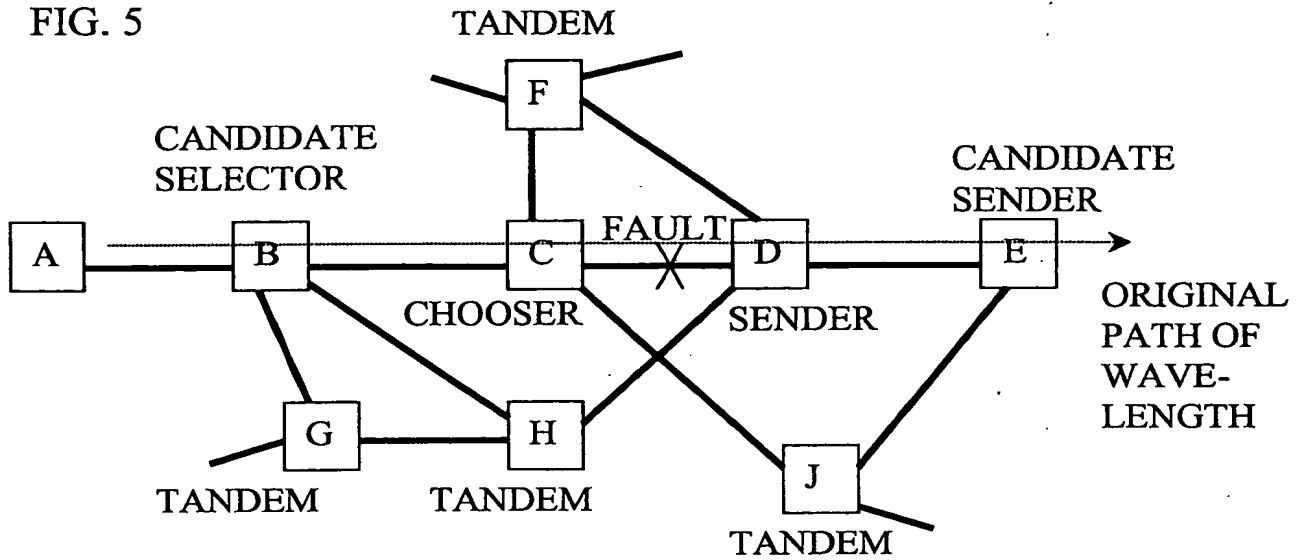


FIG. 5



ROUTE	SPARE WAVE- LENGTHS	DISPERSION	LOSS	SNR
ABGHDE	BG=3 GH=4 HD=7	BG=10 GH=5 HD=2	BG=1.3 GH=4.1 HD=2.3	BG=4 GH=3 HD=2
ABCFDE	CF=1 FD=10	CF=1 FD=3	CF=4.1 FD=3.0	CF=5 FD=10
ABCJE	CJ=4 JE=3	CJ=4 JE=3	CJ=1.1 JE=3.2	CJ=4 JE=3
ABHDE	BH=1 HD=2	BH=5 HD=6	BH=2.2 HD=4.3	BH=4 HD=5

FIG. 6

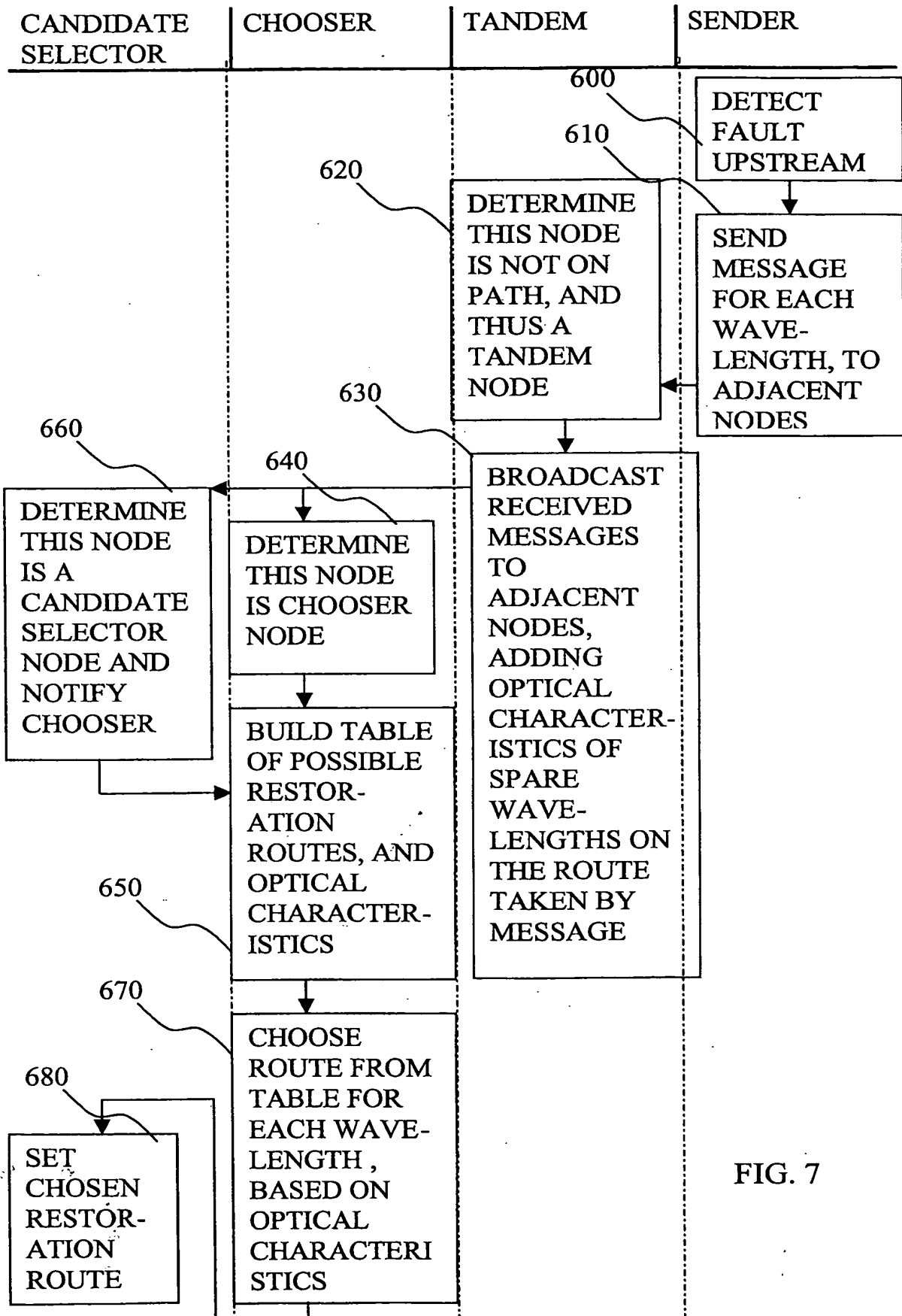


FIG. 7

FIG. 8

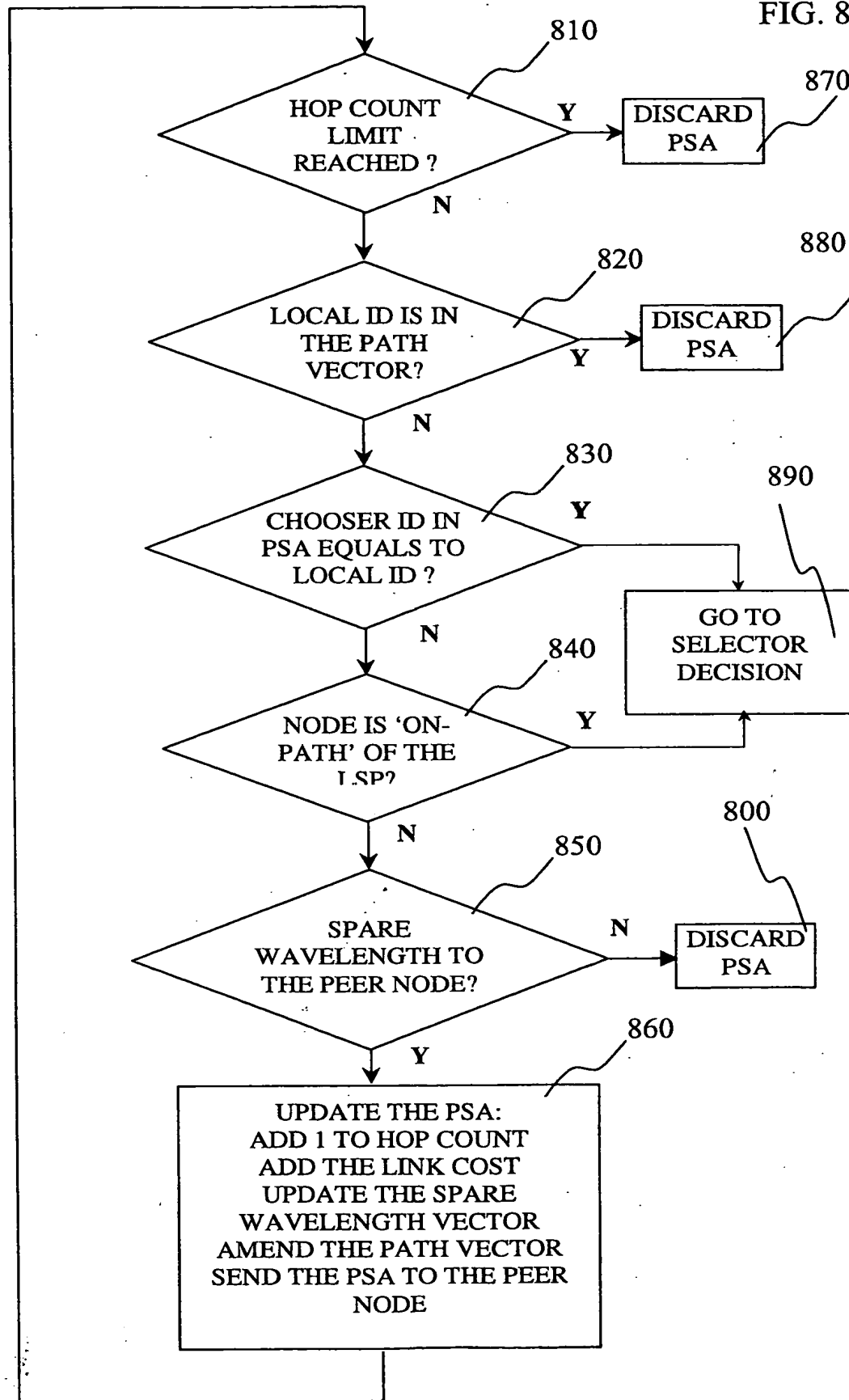
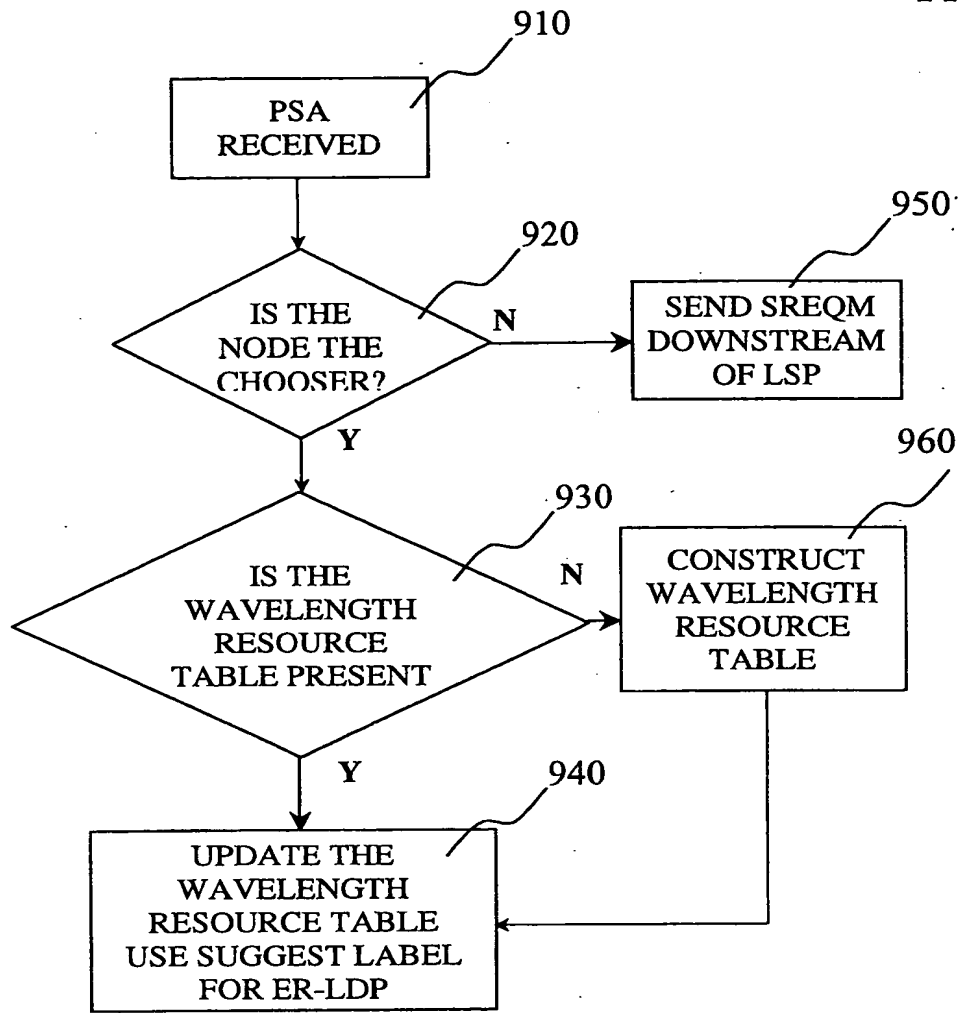


FIG. 9



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FIG. 10

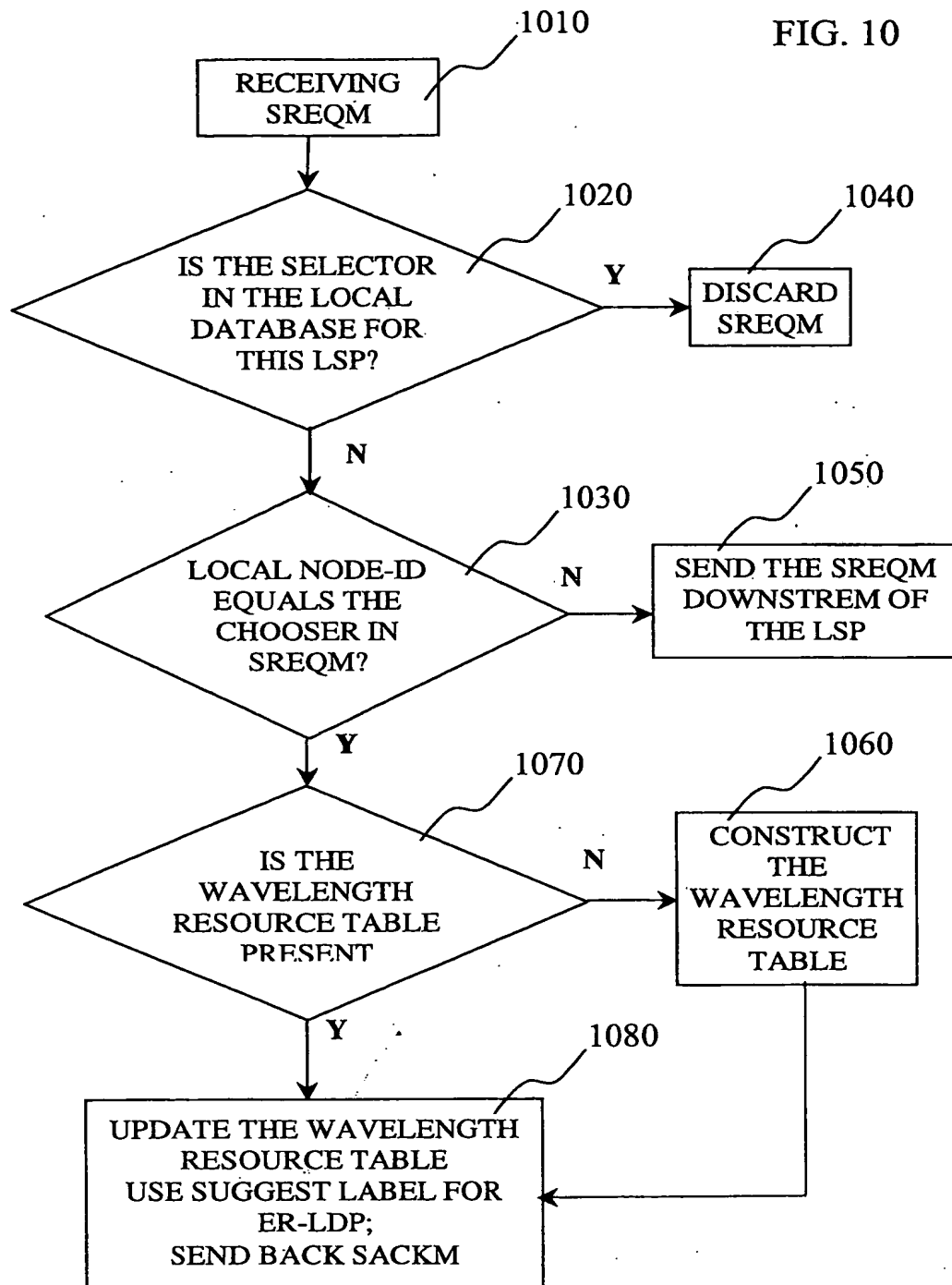


FIG. 11

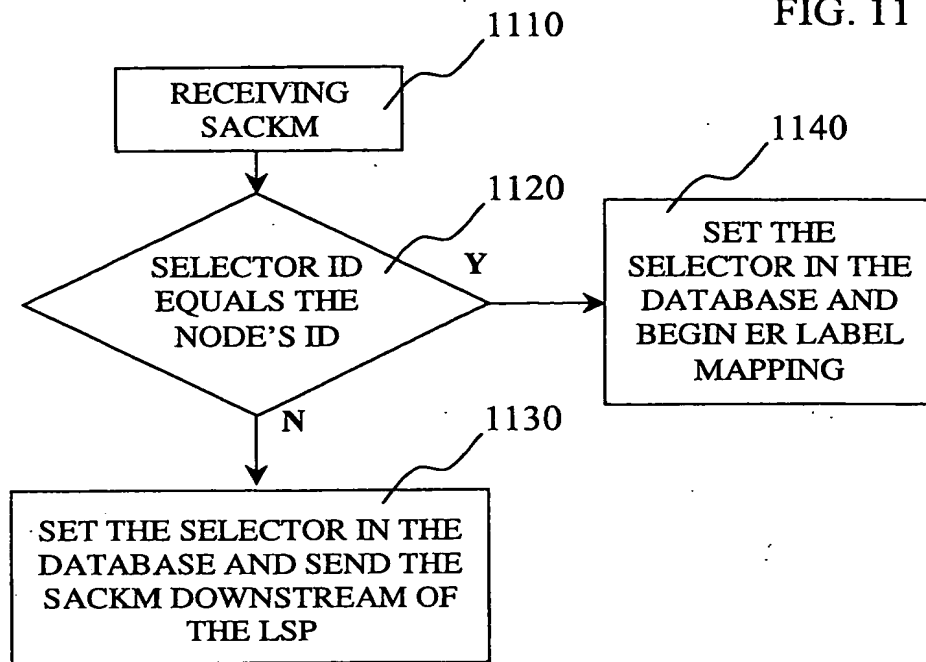


FIG. 12

